Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus comprising:

a slave access circuit coupled to one of P slave devices and K slave buses to provide access to the one of the P slave devices from one of N master processors via a system bus controller, the K slave buses being configured to couple to the P slave devices, the system bus controller interfacing to the N master processors via N master buses and dynamically mapping address spaces of the P slave devices; and

a slave bus decoder coupled to the slave access circuit to enable the one of the P slave devices to connect to one of the K slave buses when the one of the P slave devices is addressed by the one of the N master processors, the slave bus decoder being controlled by the system bus controller.

2. (original) The apparatus of claim 1 wherein the slave access circuit comprises:

K bus buffers coupled to the K slave buses to buffer bus signals corresponding to access signals to the one of the P slave devices, the K bus buffers being enabled by the slave bus decoder.

3. (original) The apparatus of claim 2 wherein each of the K bus buffers is connected to each of the K slave buses.

4-7. (canceled)

8. (currently amended) A method comprising:

providing access to one of the P slave devices from one of N master processors via a system bus controller and K slave buses, the K slave buses being configured to couple to the P slave devices, the system bus controller interfacing to the N master processors via N master buses;

dynamically mapping address spaces of the P slave devices by the bus controller;

enabling the one of the P slave devices to connect to one of the K slave buses by a slave bus decoder when the one of the P slave devices is addressed by the one of the N master processors; and

controlling the slave bus decoder by the system bus controller.

9. (original) The method of claim 8 wherein providing access comprises:

buffering bus signals corresponding to access signals to the one of the P slave devices by K bus buffers; and

enabling the K bus buffers by the slave bus decoder.

10. (original) The method of claim 9 wherein buffering the bus signals comprises:

connecting each of the K bus buffers to each of the K slave buses.

11-14. (canceled)

15. (currently amended) A system comprising:

a system bus controller coupled to N ~~bus masters~~ master processors via N master buses and K slave buses;

P slave devices; and

P slave interface circuits coupled to the P slave devices and the K slave buses, each of the P slave interface circuits comprising:

a slave access circuit coupled to one of the P slave devices and the K slave buses to provide access to the one of the P slave devices from one of the N master processors via the system bus controller, the K slave buses being configured to couple to the P slave devices, the system bus controller dynamically mapping address spaces of the P slave devices, and

a slave bus decoder coupled to the slave access circuit to enable the one of the P slave devices to connect to one of the K slave buses when the one of the P slave devices is addressed by the one of the N master processors, the slave bus decoder being controlled by the system bus controller.

16. (original) The system of claim 15 wherein the slave access circuit comprises:

K bus buffers coupled to the K slave buses to buffer bus signals corresponding to access signals to the one of the P slave devices, the K bus buffers being enabled by the slave bus decoder.

17. (original) The system of claim 16 wherein each of the K bus buffers is connected to each of the K slave buses.

18-21. (canceled)